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09/996,091	11/28/2001	Hayden Clavie Cranford JR.	RAL920010004US2 (IRA-10-5	2524

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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	6

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,091	CRANFORD ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 April 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2, 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 6, 9, 10, 11, 12, 15, 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over European Patent Application Publication Number 0 686 920 to Jeong et al. ("Jeong") in view of The Microsoft Press Computer Dictionary, 3rd Edition ("Microsoft").

3. In reference to Claim 1, Jeong teaches a method of transferring stored digital parallel data of multiple bits of data stored in a first data register from a transmitter to a receiver over a hard wired conductor (See Figure 6 Number 117) comprising the steps of: synchronously converting said stored digital data to a serial data signal in said transmitter (See Page 2 Lines 3-5 and 51-52, and Page 6 Lines 22-26); transmitting said serial signal asynchronously over said hard wired conductor to said receiver (See Figure 10, Page 2 Lines 3-5, and Page 9 Lines 9-13); and restoring said asynchronous serial signal to synchronous digital parallel data in said receiver corresponding to the

data stored in said first data register in said transmitter, including detecting both edges of the data in said asynchronous serial signal for conversion to parallel data bits (See Figure 10, Page 8 Lines 55-57, Page 9 Lines 5-13, and Page 10 Lines 17-27). Jeong does not teach converting the digital data signal to an analog data signal are restoring said analog data signal to a digital data signal. Microsoft teaches the use of a modem that converts digital signals into analog signals for transmission and converts received analog signals into digital signals (See entry 'modem').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 1, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

4. In reference to Claim 2, Jeong and Microsoft teach the limitations as applied to Claim 1 above. Jeong further teaches that the digital parallel data is read out of said first data register to at least one single bit latch (See Figure 6 Number 118 and Page 6 Lines 22-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 2, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

5. In reference to Claim 5, Jeong and Microsoft teach the limitations as applied to Claim 1 above. Jeong further teaches that the data in said first register is comprised of either eight or ten bits (See Figure 6 Numbers 116 and 117 and Page 6 Lines 32-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 5, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

6. In reference to Claim 6, Jeong and Microsoft teach the limitations as applied to Claim 1 above. Jeong further teaches that a clocking signal is used to convert said analog serial signal to a digital signal (See Page 9 Lines 5-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 6, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

7. In reference to Claim 9, Jeong and Microsoft teach the limitations as applied to Claim 1 above. Jeong further teaches that said edges are derived from multiple samples (See Page 9 Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 9, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

8. In reference to Claim 10, Jeong and Microsoft teach the limitations as applied to Claim 9 above. Jeong further teaches that said multiple samples are used to determine the approximate center of said resulting data bit (See Page 10 Lines 23-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 10, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

9. In reference to Claim 11, Jeong teaches a structure for transferring stored digital parallel data of multiple bits of data stored in a first data register, comprising a transmitter and a receiver connected by a hard wired conductor; circuitry to synchronously convert said stored digital data to a serial data signal in said transmitter (See Figure 6 Number 117); circuitry to synchronously convert said stored digital data to a serial data signal in said transmitter (See Page 2 Lines 3-5 and 51-52, and Page 6 Lines 22-26); circuitry to transmit said serial signal asynchronously over said hard wired

conductor to said receiver (See Figure 10, Page 2 Lines 3-5, and Page 9 Lines 9-13); and circuitry to restore said asynchronous serial signal to synchronous digital parallel data in said receiver corresponding to the data stored in said first data register in said transmitter, including detecting both edges of the data in said asynchronous serial signal for conversion to parallel data bits (See Figure 10, Page 8 Lines 55-57, Page 9 Lines 5-13, and Page 10 Lines 17-27). Jeong does not teach converting the digital data signal to an analog data signal are restoring said analog data signal to a digital data signal. Microsoft teaches the use of a modem that converts digital signals into analog signals for transmission and converts received analog signals into digital signals (See entry 'modem').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 11, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

10. In reference to Claim 12, Jeong and Microsoft teach the limitations as applied to Claim 11 above. Jeong further teaches including at least one single bit latch and circuitry to read the digital parallel data out of said first data register to said at least one single bit latch (See Figure 6 Number 118 and Page 6 Lines 22-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft,

resulting in the invention of Claim 12, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

11. In reference to Claim 15, Jeong and Microsoft teach the limitations as applied to Claim 11 above. Jeong further teaches that the data in said first register is comprised of either eight or ten bits (See Figure 6 Numbers 116 and 117 and Page 6 Lines 32-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 15, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

12. In reference to Claim 16, Jeong and Microsoft teach the limitations as applied to Claim 11 above. Jeong further teaches a clocking signal to convert said analog serial signal to a digital signal (See Page 9 Lines 5-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 16, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

13. In reference to Claim 19, Jeong and Microsoft teach the limitations as applied to Claim 11 above. Jeong further teaches circuitry to derive said edges from multiple samples (See Page 9 Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 19, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

14. In reference to Claim 20, Jeong and Microsoft teach the limitations as applied to Claim 19 above. Jeong further teaches circuitry to derive said edges from said multiple samples determines the approximate center of said resulting data bit (See Page 10 Lines 23-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong with the modem of Microsoft, resulting in the invention of Claim 20, in order to allow the device, which is digital, to transmit data over, and receive data from, a standard telephone line, which is analog (see entry 'modem' in Microsoft).

15. Claims 3, 4, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong and Microsoft as applied to Claims 2 and 12 above, and further in view of US Patent Number 6,222,380 to Gerowitz et al. ("Gerowitz").

16. In reference to Claim 3, Jeong and Microsoft teach the limitations as applied to Claim 2 above. Jeong and Microsoft do not teach that the data is read out from said first register in said transmitter two bits at a time, each data bit to first and second single data bit registers, and from each first and second single bit data register to a third single bit data register, clocking additional two data bits to be subsequently written to said first and second one bit registers and to said third single bit data register until all bits of the data have been read from the first register. Gerowitz teaches reading out data into N registers, which includes the 2 registers as claimed (See Figure 2 and Column 4 Lines 36-37); and reading out data from the N registers into a single register (See Figure 2 and Column 4 Lines 38-41). The device of Gerowitz will inherently clock an additional N bits into the N registers until all of the data have been read.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong and Microsoft with the parallel to serial conversion device of Gerowitz, resulting in the invention of Claim 3, in order to allow the data to be transmitted over a high-speed, high-volume data path that uses fewer pins and transfers data at a faster rate than a traditional bus structure (See Column 2 Lines 16-20).

17. In reference to Claim 4, Jeong, Microsoft, and Gerowitz teach the limitations as applied to Claim 3 above. Gerowitz further teaches converting the bits from the third register to a single serial signal of the data (See Figure 2 and Column 4 Lines 40-42).

As in Claim 1 above, Microsoft teaches the use of a modem that converts digital signals into analog signals (See entry 'modem').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong and Microsoft with the parallel to serial conversion device of Gerowitz, resulting in the invention of Claim 4, in order to allow the data to be transmitted over a high-speed, high-volume data path that uses fewer pins and transfers data at a faster rate than a traditional bus structure (See Column 2 Lines 16-20).

18. In reference to Claim 13, Jeong and Microsoft teach the limitations as applied to Claim 12 above. Jeong and Microsoft do not teach first, second and third single data bit registers, and wherein the data is read out from said first register in said transmitter two bits at a time, each data bit to either said first or second single data bit registers, and then from each first and second single bit data register to said third single bit data register, clocking to clock additional two data bits to be subsequently written to said first and second one bit registers and to said third single bit data register until all bits of the data have been read from the first register. Gerowitz teaches reading out data into N registers, which includes the 2 registers as claimed (See Figure 2 and Column 4 Lines 36-37); and reading out data from the N registers into a single register (See Figure 2 and Column 4 Lines 38-41). The device of Gerowitz will inherently clock an additional N bits into the N registers until all of the data have been read.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong and Microsoft with the parallel to serial conversion device of Gerowitz, resulting in the invention of Claim 13, in order to allow the data to be transmitted over a high-speed, high-volume data path that uses fewer pins and transfers data at a faster rate than a traditional bus structure (See Column 2 Lines 16-20).

19. In reference to Claim 14, Jeong, Microsoft, and Gerowitz teach the limitations as applied to Claim 13 above. Gerowitz further teaches circuitry to convert the bits from the third single bit register into a single analog serial signal of the data (See Figure 2 and Column 4 Lines 40-42). As in Claim 11 above, Microsoft teaches the use of a modem that converts digital signals into analog signals (See entry 'modem').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong and Microsoft with the parallel to serial conversion device of Gerowitz, resulting in the invention of Claim 14, in order to allow the data to be transmitted over a high-speed, high-volume data path that uses fewer pins and transfers data at a faster rate than a traditional bus structure (See Column 2 Lines 16-20).

20. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong, Microsoft, and Gerowitz as applied to Claim 3 above, and further in view of US Patent Number 5,202,979 to Hillis et al. ("Hillis").

21. In reference to Claim 7, Jeong and Microsoft teach the limitations as applied to Claim 3 above. Jeong and Microsoft do not teach said analog signal is converted in said receiver to two one-bit signals and delivered to a shift register and then stored in a second data register. Jeong further teaches storing the converted bits in said second data register (See Figure 10). Hillis teaches a shift register that takes two bits from an input signal and shifts them two bits at every clock pulse before shifting the accumulated bits out in parallel (See Figure 3 Number 34 and Column 3 Line 49 – Column 4 Line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong and Microsoft with the 2 bit shift register of Hillis, resulting in the invention of Claim 7, in order to speed up data transfer by only needing half as many clock pulses to accumulate the data from the input line (See Column 4 Lines 8-10 of Hillis), as well as to reduce power consumption since fewer clock transitions are required.

22. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong, Microsoft, and Hillis as applied to Claim 17 above, and further in view of Newton's Telecom Dictionary, 8th Edition ("Newton").

23. In reference to Claim 8, Jeong, Microsoft, and Hillis teach the limitations as applied to Claim 7 above. Jeong, Microsoft, and Hillis do not teach that said bits in the

shift register are delivered synchronously from said shift register to said second data register. Newton teaches the use of synchronous transmission (See entry 'Synchronous Transmission').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong, Microsoft, and Hillis with the synchronous transmission of Newton, resulting in the invention of Claim 8, because synchronous transmission eliminated the need for start and stop bits (See entry 'Synchronous Transmission' in Newton).

24. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong and Microsoft as applied to Claim 11 above, and further in view of Hillis.

25. In reference to Claim 17, Jeong and Microsoft teach the limitations as applied to Claim 11 above. Jeong and Microsoft do not teach a second data bit register and circuitry in said receiver to convert said analog signal to two one-bit signals delivered to a shift register. Jeong further teaches storing the converted bits in said second data register (See Figure 10). Hillis teaches a shift register that takes two bits from an input signal and shifts them two bits at every clock pulse before shifting the accumulated bits out in parallel (See Figure 3 Number 34 and Column 3 Line 49 – Column 4 Line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong and Microsoft with the 2 bit shift register of Hillis, resulting in the invention of Claim 17, in order to speed up data transfer

by only needing half as many clock pulses to accumulate the data from the input line (See Column 4 Lines 8-10 of Hillis), as well as to reduce power consumption since fewer clock transitions are required.

26. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong, Microsoft, and Hillis as applied to Claim 17 above, and further in view of Newton.

27. In reference to Claim 18, Jeong, Microsoft, and Hillis teach the limitations as applied to Claim 17 above. Jeong, Microsoft, and Hillis do not teach that said bits in the shift register are delivered synchronously from said shift register to said second data register. Newton teaches the use of synchronous transmission (See entry 'Synchronous Transmission').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jeong, Microsoft, and Hillis with the synchronous transmission of Newton, resulting in the invention of Claim 18, because synchronous transmission eliminated the need for start and stop bits (See entry 'Synchronous Transmission' in Newton).

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 5,069,522 to Block et al. ("Block") teaches a

system that converts parallel data to serial data and transmits it asynchronously to a receiver which then converts the serial data back to parallel data (See Figure 4).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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